REMARKS

Claims 1, 2, 7, 9, 12-14, 27, and 37 are pending in the application.

Claims 1, 2, 13, 14, and 27 are currently amended; claims 3-6, 8, 10, 11, and 15-26 are canceled; and new claim 37 is added. Applicants respectfully submit that no new matter is added to currently amended claims 1, 2, 7, 9, 12-14, and 27 or to new claim 37.

Applicant respectfully submits that entry of the currently amended claims is proper because the currently amended claims will either place the application in condition for allowance or in better form for appeal.

Claims 7 and 27 stand rejected under 35 U.S.C. §112, second paragraph, and claim 13 stands rejected under U.S.C. §112, first paragraph.

Claims 1 and 14 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,506,642 to Luning.

Claims 2 and 6 stand rejected under 35 U.S.C. §103(a) as unpatentable over Luning, in view of U.S. Patent No. 6,258,680 to Fulford.

Claims 7 and 27 stand rejected under 35 U.S.C. §103(a) as unpatentable over Luning, in view of Fulford, and further in view of U.S. Patent No. 5,882,973 to Gardner.

Claims 9 and 12 stand rejected under 35 U.S.C. §103(a) as unpatentable over Luning, in view of U.S. Patent No. 6,730,556 to Wu.

Applicants respectfully traverse the rejections based on the following discussion.

I. The 35 U.S.C. §112 Rejections

Claims 7 and 27 stand rejected under 35 U.S.C. §112, second paragraph, because, as the Office Action points out, Fig. 8 illustrates the silicide regions being formed on the oxide layer 106, whereas the Specification, at paragraphs 31 and 38, states the silicide being formed on the exposed areas of the substrate. The Office Action has interpreted the claims in light of Fig. 8.

Applicants would also like the claims to be interpreted in light of Fig. 8. Hence, Applicants propose amending paragraphs 31 and 38 of the Specification, above, in order to bring Fig. 8 and the Specification into congruence.

Claim 13 stand rejected under 35 U.S.C. §112, first paragraph, because, as the Office Action points out, the Specification does not describe the oxide layer as a low temperature oxide (LTO). Instead, the specification recites that the etch stop layer is a low temperature oxide.

Applicants have currently amended claim 13 to recite in relevant part, "wherein said etch stop layer comprises a low temperature oxide".

For at least the reasons outlined above, Applicants respectfully submit that claims 7 and 27 particularly point out and distinctly claim the subject matter, as described in the currently amended Specification, which Applicants regard as the invention, and that claim 13, as currently amended, is enabled. Withdrawal of the rejection of claims 7 and 27 under 35 U.S.C. §112, second paragraph, and claim 13 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

II. The Prior Art Rejections

A. The 35 U.S.C. 102(b) Rejection over Luning

1. The Luning Disclosure

As illustrated in Fig. 4, Luning discloses first and second transistors, i.e., n-MOS and p-MOS transistors of a CMOS device, typically separated by a trench isolation containing silicon oxide fill. First gate electrode 41 is formed over a semiconductor substrate 40 with first gate dielectric layer 43A therebetween in the n-MOS region, and a second gate electrode 42 is formed over substrate 40 with second gate dielectric layer 43B therebetween in the p-MOS region. Shallow source/drain extensions 45, 46 are then formed in a conventional manner employing gate electrodes 41 and 42 as masks. Subsequently, the first sidewall spacer is deposited on the side surface of the first and second gate electrodes 41, 42. (col. 4, lines 36-49).

As illustrated in Fig. 5, Luning also discloses that a photoresist mask is formed over the second gate electrode 42, inclusive of the first sidewall spacers 44, and etching is conducted to remove the first sidewall spacers 44 from the side surfaces of the first gate electrode 41. As further shown in Fig. 6, a second sidewall spacer deposited on the side surfaces of the first gate electrode 41 and on the first sidewall spacers 44 positioned on the side surfaces of the second gate electrode 42.

Luning further discloses that in Fig. 6, the width of the second sidewall spacer W_2

selectively controls the length of the source/drain extension 46 of the N-MOS transistor, while the thickness of the first and second sidewalls W_3, typically about 900 Å to 1,500 Å, controls the length of the source/drain extension of p-MOS transistor.

2. Arguments

Currently amended, independent claim 1 recites in relevant part,

"an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers".

While the Office Action asserts that Fig. 6 of Luning discloses the "first impurity source/drain implant region 61 formed in said substrate [is] substantially adjacent to outer edges of said first spacer" (page 4, lines 2 and 3) and that the "second impurity source/drain implant region [62], formed in said substrate, [is] substantially adjacent to outer edges of said second spacer" (page 4, lines 7-9), Luning, in fact, contradicts this disclosure by stating, "the width of the second sidewall spacer W_2 selectively controls the length of the source/drain extension 46 of the N-MOS transistor, while the thickness of the first and second sidewalls W_3, typically about 900 Å to 1,500 Å, controls the length of the source/drain extension of p-MOS transistor". (emphasis added). In fact, Luning never explicitly describes regions 61 and 62 of Fig. 6 in the Description of the Invention, and instead, explicitly describes only the shallow source/drain extensions 45, 46.

The present invention clearly describes at least the features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", in which in currently amended, independent claim 1.

In contrast, nowhere does Luning disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers".

Instead, Luning merely discloses that a second sidewall spacer may be deposited on the side surfaces of the first gate electrode 41 and on the first sidewall spacers 44 positioned on the side surfaces of the second gate electrode 42. Luning does not disclose, teach or suggest an etch

stop layer interposed between the first and second sidewall spacers.

For at least the reasons outlined above, Applicants respectfully submit that Luning does not disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently amended, independent claim 1. Accordingly, Luning fails to anticipate the subject matter of currently amended, independent claim 1 and dependent claim14 under 35 U.S.C. §102(b). Withdrawal of the rejection of claims 1 and 14 under 35 U.S.C. §102(b) over Luning is respectfully solicited.

B. The 35 U.S.C. 103(a) Rejection over Luning and Fulford

1. The Fulford Disclosure

Fig. 6 of Fulford discloses that an oxide layer 128 is grown upon semiconductor substrate 110, upon upper surfaces 116 and 120 of gate conductor 114 by oxidizing the silicon in those areas. Oxide layer 128 is to act as an etch stop during subsequent formation and removal of a spacer material set forth below. (col. 8, lines 13-19).

Fulford also discloses in Fig. 9 that an oxide layer 146 may be deposited upon the semiconductor topography. Oxide layer 128 is preferably deposited using a CVD process. If desired, an anisotropic etch may be used to remove the oxide from substantially horizontal surfaces. Resulting from deposition and possible etch, oxide layer 146 is formed above gate conductor 114 and immediately adjacent spacers 136 and 138 as oxide spacers 148 and 150. (col. 8, lines 49-56).

Fig. 11 (and Fig. 12) of Fulford disclose a conformal layer 158, that is anisotropically etched, preferably using a plasma etch process, until layer 158 is cleared from the substantially horizontal planar regions of oxide layer 128 and oxide layer 146. By using an anisotropic etch and minimizing the overetch, spacer structures 160 and 162 are formed on the exterior sidewall surfaces of oxide spacers 148 and 150. The spacers are preferably nitride or polysilicon, which extend a horizontal distance d_3 from opposing sidewall surfaces 116 and 120 of gate conductor 114, respectively. col. 9, lines 4-14).

2. Arguments

Claim 6 is presently canceled; hence, the rejection of claim 6 over Luning and Fulford is moot.

However, as a convenience to the Examiner, the following discussion presents Applicant's arguments with respect to the subject matter of claim 6, which has been incorporated into independent claim 1.

Currently amended, independent claim 1 recites in relevant part,

"an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers".

The Office Action states, "Fulford teaches in Fig 12 that an etch stop layer is formed directly on said oxide layer (150 formed directly on 128) formed directly on said sidewalls of said PFET gate conductor to act as an etch stop so that a second set of nitride spacer can be formed (col. 9, line 4-12).

Applicants respectfully submit that the Office Action has misconstrued Fulford.

Fulford clearly describes, "Oxide layer 128 is to act as an etch stop during subsequent formation and removal of a spacer material … .", (col. 8, lines 13-19); and "oxide layer 146 is formed above gate conductor 114 and immediately adjacent spacers 136 and 138 as oxide spacers 148 and 150.", (col. 8, lines 49-56). Thus, Fig. 12 illustrates, on the right side of the structure, (1) oxide layer 128, which acts as an etch stop; (2) a nitride spacer, 138; (3) an oxide spacer, 150; and (4) a nitride spacer 162. Therefore, 150, an oxide layer, is not identified as the etch stop layer; instead, oxide layer 128 is described as the etch stop layer. Hence, the Office Action's assertion that an etch stop layer, 150, is formed on an oxide layer, 128, is incorrect.

In addition, Applicants respectfully submit that Fulford does not cure the deficiencies of Luning argued above. That is, nowhere does Fulford disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers ", as recited in currently amended, independent claim 1.

Instead, Fulford describes: oxide layer 128, which acts as an etch stop; upon which a nitride spacer, 138, is formed; further upon which, an oxide spacer, 150, is formed; and yet further upon which, a nitride spacer 162, is formed.

For at least the reasons outlined above with respect to the rejection of the claims over Luning, and for at least the reasons outlined immediately above with respect to Fulford, Applicants respectfully submit that Luning and Fulford, either independently or in combination, do not disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently amended, independent claim 1. Accordingly, Luning and Fulford, either independently or in combination, fail to render obvious the subject matter of currently amended, independent claim 1 and dependent claim 2 under 35 U.S.C. §103(a). The rejection of canceled claim 6 is moot. Withdrawal of the rejection of claim 6 under 35 U.S.C. §103(a) over Luning and Fulford is respectfully solicited.

C. The 35 U.S.C. 103(a) Rejection over Luning, Fulford, and Gardner

1. The Gardner Disclosure

Fig. 7 of Gardner illustrates salicidation of exposed silicon-based surfaces. (col. 7, lines 57 and 58).

2. Arguments

Currently amended, independent claim 1 recites in relevant part,

"an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers".

Gardner merely discloses that exposed silicon-based layers may be salicided.

However, Gardner does not cure the deficiencies of Luning and Fulford argued above.

Applicants respectfully submit that nowhere does Gardner disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently

amended, independent claim 1.

Instead, Gardner merely discloses that exposed silicon-based layers may be salicided.

For at least the reasons outlined above with respect to the rejection of the claims over Luning and Fulford, and for at least the reasons outlined immediately above with respect to Gardner, Applicants respectfully submit that Luning, Fulford and Gardner, either independently or in combination, do not disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently amended, independent claim 1. Accordingly, Luning, Fulford and Gardner, either independently or in combination, fail to render obvious the subject matter of currently amended, independent claim 1 and dependent claims 7 and 27 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 7 and 27 under 35 U.S.C. §103(a) over Luning, Fulford and Gardner is respectfully solicited.

D. The 35 U.S.C. 103(a) Rejection over Luning and Wu

1. The Wu Disclosure

Wu discloses that an n-type dopant may be arsenic (col. 1, line 64) and a p-type dopant may be boron (col. 2, line 2).

2. Arguments

Currently amended, independent claim 1 recites in relevant part,

"an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers".

Wu merely discloses that an n-type dopant may be arsenic and a p-type dopant may be boron.

However, Wu does not cure the deficiencies of Luning argued above.

Applicants respectfully submit that nowhere does Wu disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently amended,

independent claim 1.

Instead, Wu merely discloses that an n-type dopant may be arsenic and a p-type dopant may be boron.

For at least the reasons outlined above with respect to the rejection of claim 1 over Luning, and for at least the reasons outlined immediately above with respect to Wu, Applicants respectfully submit that Luning and Wu, either independently or in combination, do not disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in currently amended, independent claim 1. Accordingly, Luning and Wu, either independently or in combination, fail to render obvious the subject matter of currently amended, independent claim 1 and dependent claims 9 and 12 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 9 and 12 under 35 U.S.C. §103(a) over Luning and Wu is respectfully solicited.

III. Formal Matters and Conclusion

Claims 1, 2, 7, 9, 12-14, 27, and 37 are pending in the application.

Applicants respectfully submit that claims 7, 13, and 27 satisfy the statutory requirements of 35 U.S.C. §112, first and second paragraphs, for the reasons outlined above.

With respect to the rejections of the claims over the cited prior art, Applicants respectfully submit that the present claims are distinguishable over the prior art of record. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1, 2, 7, 9, 12-14, 27, and 37 all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest time possible.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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